EAST - [Untitled1:1]

File View Edit Tools Window Help

L7: (20) 6 and (implant$3 near (sidewall or trench or opening or wall))
L8: (251) 4 and (node near (storage or dielectric))
L9: (38) 8 and (remov$3 near (insulat$3 or dielectric))
L10: (38) 9 and (implant$3)
L11: (210) tews.in.
L12: (202) collar near dielectric
L13: (119) 12 and (trench$2)
L14: (117) 13 and (capacitor or node or storage)
L15: (69) 14 and (implant$3)
L16: (2) 15 and (implant$3 near (trench or top or upper or dielectric))
Failed
Saved

Browse | Queue | Clear
DBs | USPAT;US-PGPUB | Bursts
Default operator: OR | Highlight all hit terms nearby

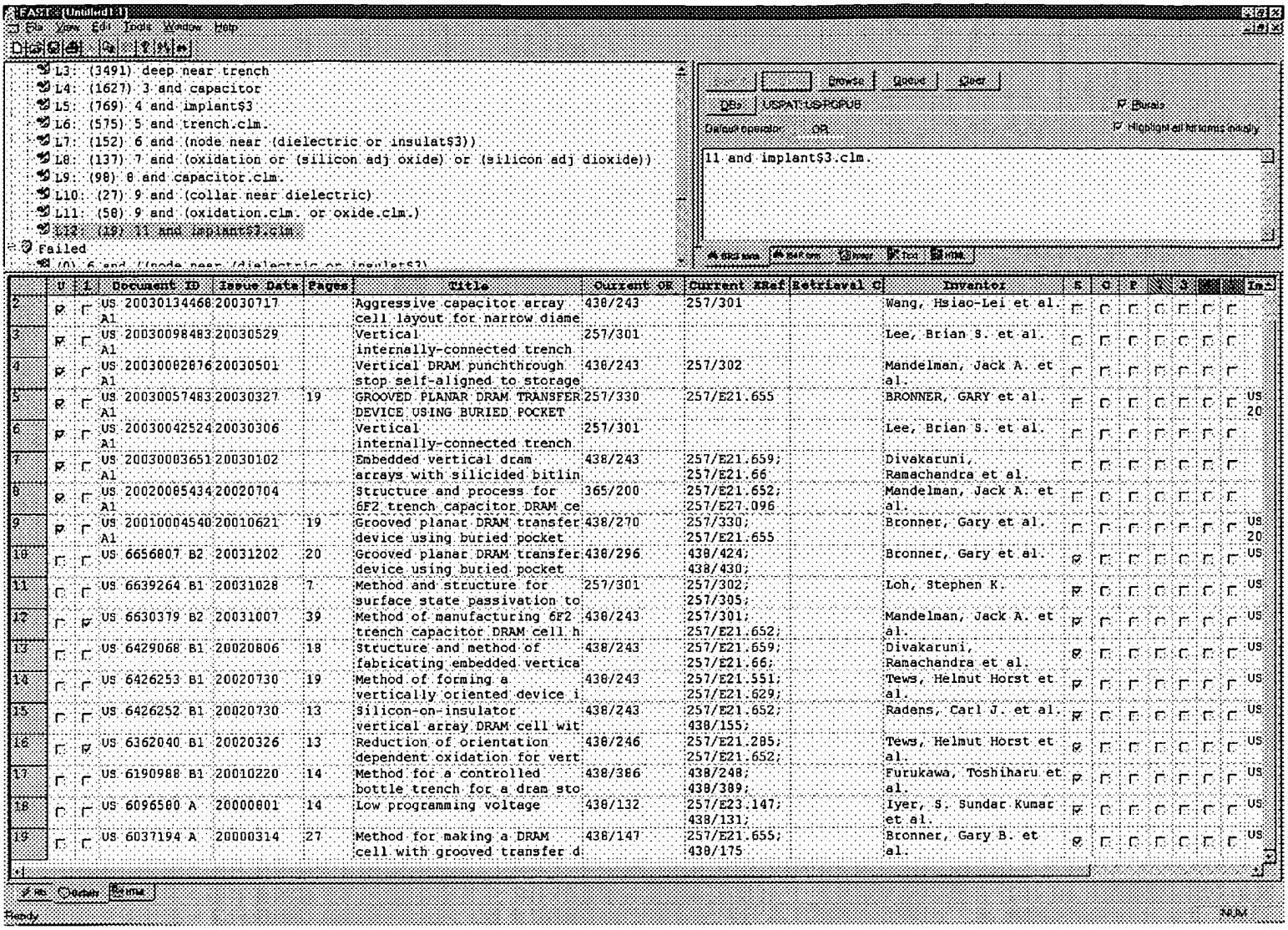
9 and (implant$3)

Edit term | Add term | Image | Text | Hits

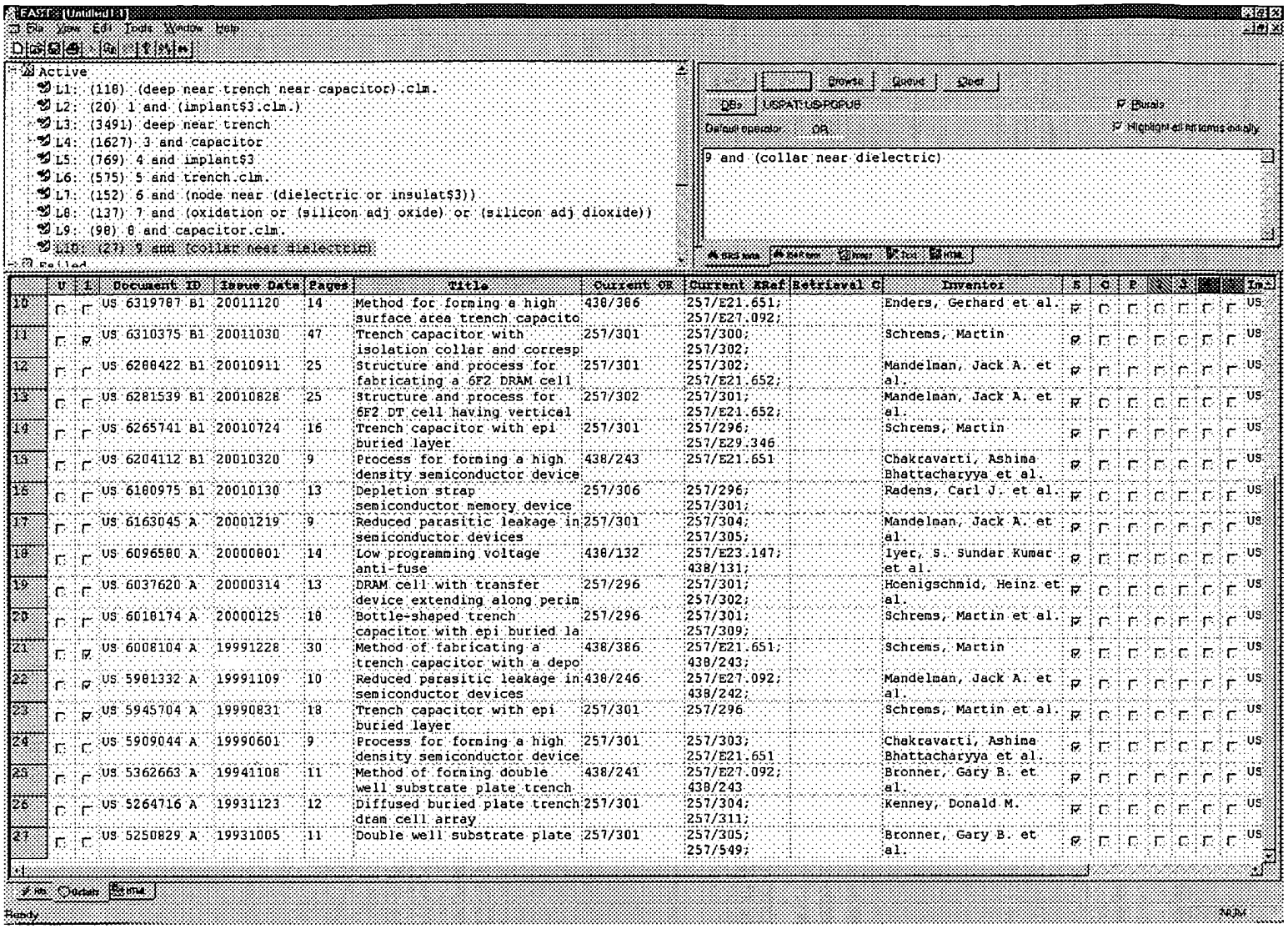
	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P					In
7	☐	☐	US 6420750 B1	20020716	10	Structure and method for buried-strap with reduced ou	257/302	257/327; 257/E21.653;		Divakaruni, Ramachandra et al.	☑	☐	☐	☐	☐	☐	☐	US
8	☐	☐	US 6417063 B1	20020709	20	Folded deep trench capacitor and method	438/386	257/E21.651; 438/243;		Petter, Robert et al.	☑	☐	☐	☐	☐	☐	☐	US
9	☐	☑	US 6319700 B1	20011120	35	Semiconductor structure and manufacturing methods	438/386	257/296; 257/E21.396		Gruening, Ulrike et al.	☑	☐	☐	☐	☐	☐	☐	US
10	☐	☑	US 6310375 B1	20011030	47	Trench capacitor with isolation collar and corresp	257/301	257/300; 257/302;		Schrems, Martin	☑	☐	☐	☐	☐	☐	☐	US
11	☐	☐	US 6284665 B1	20010904	10	Method for controlling the shape of the etch front in t	438/710	257/E21.312; 257/E21.396;		Lill, Thorsten et al.	☑	☐	☐	☐	☐	☐	☐	US
12	☐	☐	US 6281539 B1	20010828	25	Structure and process for 6f2 DT cell having vertical	257/302	257/301; 257/E21.652;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
13	☐	☐	US 6265742 B1	20010724	17	Memory cell structure and fabrication	257/304	257/302; 257/303;		Gruening, Ulrike et al.	☑	☐	☐	☐	☐	☐	☐	US
14	☐	☑	US 6265741 B1	20010724	16	Trench capacitor with epi buried layer	257/301	257/296; 257/E29.346		Schrems, Martin	☑	☐	☐	☐	☐	☐	☐	US
15	☐	☐	US 6242310 B1	20010605	10	Method of forming buried-strap with reduced ou	438/268	257/E21.653; 438/269;		Divakaruni, Ramachandra et al.	☑	☐	☐	☐	☐	☐	☐	US
16	☐	☐	US 6204112 B1	20010320	9	Process for forming a high density semiconductor device	438/243	257/E21.651		Chakravarti, Ashima Bhattacharyya et al.	☑	☐	☐	☐	☐	☐	☐	US
17	☐	☐	US 6190980 B1	20010220	14	Method for a controlled bottle trench for a dram sto	438/386	438/248; 438/389;		Furukawa, Toshiharu et al.	☑	☐	☐	☐	☐	☐	☐	US
18	☐	☐	US 6184151 B1	20010206	26	Method for forming cornered images on a substrate and ph	438/743	257/E21.035; 257/E21.036;		Adair, William J. et al.	☑	☐	☐	☐	☐	☐	☐	US
19	☐	☐	US 6180975 B1	20010130	13	Depletion strap semiconductor memory device	257/306	257/296; 257/301;		Radens, Carl J. et al.	☑	☐	☐	☐	☐	☐	☐	US
20	☐	☐	US 6163045 A	20001219	9	Reduced parasitic leakage in semiconductor devices	257/301	257/304; 257/305;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
21	☐	☐	US 6093614 A	20000725	10	Memory cell structure and fabrication	438/388	257/E21.652; 257/E27.096;		Gruening, Ulrike et al.	☑	☐	☐	☐	☐	☐	☐	US
22	☐	☐	US 6074954 A	20000613	18	Process for control of the shape of the etch front in t	438/710	257/E21.312; 257/E21.396;		Lill, Thorsten et al.	☑	☐	☐	☐	☐	☐	☐	US
23	☐	☐	US 6040213 A	20000321	13	Polysilicon mini spacer for trench buried strap formatio	438/243	257/E21.651; 438/246		Canale, Anthony J. et al.	☑	☐	☐	☐	☐	☐	☐	US
24	☐	☐	US 6022781 A	20000208	10	Method for fabricating a MOSFET with raised STI isola	438/296	257/301; 257/305;		Noble, Jr., Wendell P. et al.	☑	☐	☐	☐	☐	☐	☐	US

Ready

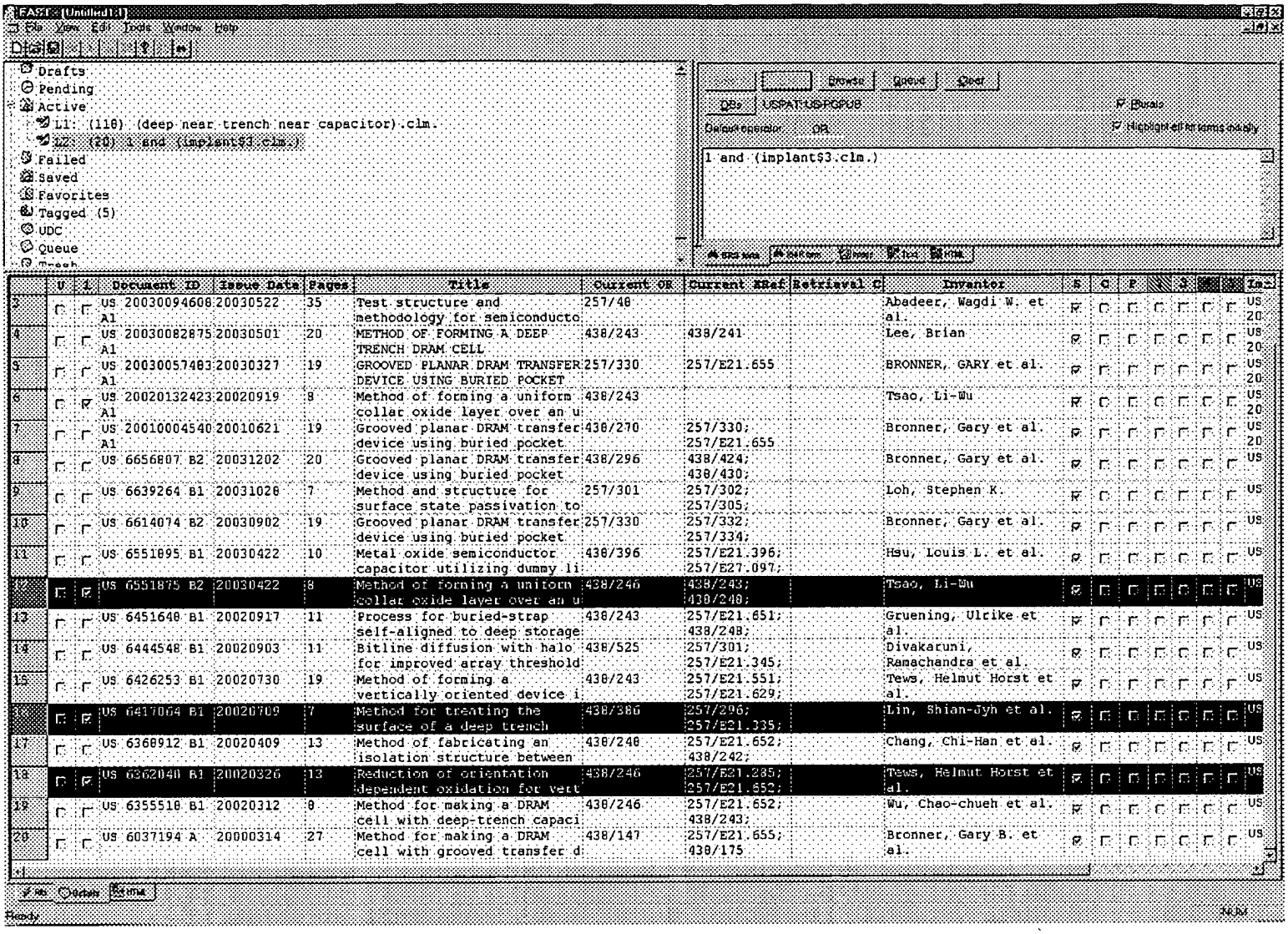
NUM



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P					In
2	☑	☐	US 20030134460 A1	20030717		Aggressive capacitor array cell layout for narrow diame	438/243	257/301		Wang, Hsiao-Lei et al.	☐	☐	☐	☐	☐	☐	☐	
3	☑	☐	US 20030098483 A1	20030529		Vertical internally-connected trench	257/301			Lee, Brian S. et al.	☐	☐	☐	☐	☐	☐	☐	
4	☑	☐	US 20030082876 A1	20030501		Vertical DRAM punchthrough stop self-aligned to storage	438/243	257/302		Mandelman, Jack A. et al.	☐	☐	☐	☐	☐	☐	☐	
5	☑	☐	US 20030057483 A1	20030327	19	GROOVED PLANAR DRAM TRANSFER DEVICE USING BURIED POCKET	257/330	257/E21.655		BRONNER, GARY et al.	☐	☐	☐	☐	☐	☐	☐	US 20
6	☑	☐	US 20030042524 A1	20030306		Vertical internally-connected trench	257/301			Lee, Brian S. et al.	☐	☐	☐	☐	☐	☐	☐	
7	☑	☐	US 20030003651 A1	20030102		Embedded vertical dram arrays with silicided bitlin	438/243	257/E21.659; 257/E21.66		Divakaruni, Ramachandra et al.	☐	☐	☐	☐	☐	☐	☐	
8	☑	☐	US 20020065434 A1	20020704		Structure and process for 6F2 trench capacitor DRAM ce	365/200	257/E21.652; 257/E27.096		Mandelman, Jack A. et al.	☐	☐	☐	☐	☐	☐	☐	
9	☑	☐	US 20010004540 A1	20010621	19	Grooved planar DRAM transfer device using buried pocket	438/270	257/330; 257/E21.655		Bronner, Gary et al.	☐	☐	☐	☐	☐	☐	☐	US 20
10	☐	☐	US 6656807 B2	20031202	20	Grooved planar DRAM transfer device using buried pocket	438/296	438/424; 438/430;		Bronner, Gary et al.	☑	☐	☐	☐	☐	☐	☐	US
11	☐	☐	US 6639264 B1	20031028	7	Method and structure for surface state passivation to	257/301	257/302; 257/305;		Loh, Stephen K.	☑	☐	☐	☐	☐	☐	☐	US
12	☐	☑	US 6630379 B2	20031007	39	Method of manufacturing 6F2 trench capacitor DRAM cell h	438/243	257/301; 257/E21.652;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
13	☐	☐	US 6429068 B1	20020806	18	Structure and method of fabricating embedded vertica	438/243	257/E21.659; 257/E21.66;		Divakaruni, Ramachandra et al.	☑	☐	☐	☐	☐	☐	☐	US
14	☐	☐	US 6426253 B1	20020730	19	Method of forming a vertically oriented device i	438/243	257/E21.551; 257/E21.629;		Tews, Helmut Horst et al.	☑	☐	☐	☐	☐	☐	☐	US
15	☐	☐	US 6426252 B1	20020730	13	Silicon-on-insulator vertical array DRAM cell wit	438/243	257/E21.652; 438/155;		Radens, Carl J. et al.	☑	☐	☐	☐	☐	☐	☐	US
16	☐	☑	US 6362040 B1	20020326	13	Reduction of orientation dependent oxidation for vert	438/246	257/E21.285; 257/E21.652;		Tews, Helmut Horst et al.	☑	☐	☐	☐	☐	☐	☐	US
17	☐	☐	US 6190988 B1	20010220	14	Method for a controlled bottle trench for a dram sto	438/386	438/248; 438/389;		Furukawa, Toshiharu et al.	☑	☐	☐	☐	☐	☐	☐	US
18	☐	☐	US 6096580 A	20000801	14	Low programming voltage	438/132	257/E23.147; 438/131;		Iyer, S. Sundar Kumar et al.	☑	☐	☐	☐	☐	☐	☐	US
19	☐	☐	US 6037194 A	20000314	27	Method for making a DRAM cell with grooved transfer d	438/147	257/E21.655; 438/175		Bronner, Gary B. et al.	☑	☐	☐	☐	☐	☐	☐	US



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P					In
10	☐	☐	US 6319787 B1	20011120	14	Method for forming a high surface area trench capacito	438/386	257/E21.651; 257/E27.092;		Enders, Gerhard et al.	☑	☐	☐	☐	☐	☐	☐	US
11	☐	☑	US 6310375 B1	20011030	47	Trench capacitor with isolation collar and corresp	257/301	257/300; 257/302;		Schrems, Martin	☑	☐	☐	☐	☐	☐	☐	US
12	☐	☐	US 6288422 B1	20010911	25	Structure and process for fabricating a 6F2 DRAM cell	257/301	257/302; 257/E21.652;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
13	☐	☐	US 6281539 B1	20010828	25	Structure and process for 6F2 DT cell having vertical	257/302	257/301; 257/E21.652;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
14	☐	☐	US 6265741 B1	20010724	16	Trench capacitor with epi buried layer	257/301	257/296; 257/E29.346		Schrems, Martin	☑	☐	☐	☐	☐	☐	☐	US
15	☐	☐	US 6204112 B1	20010320	9	Process for forming a high density semiconductor device	438/243	257/E21.651		Chakravarti, Ashima Bhattacharyya et al.	☑	☐	☐	☐	☐	☐	☐	US
16	☐	☐	US 6100975 B1	20010130	13	Depletion strap semiconductor memory device	257/306	257/296; 257/301;		Radens, Carl J. et al.	☑	☐	☐	☐	☐	☐	☐	US
17	☐	☐	US 6163045 A	20001219	9	Reduced parasitic leakage in semiconductor devices	257/301	257/304; 257/305;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
18	☐	☐	US 6096580 A	20000801	14	Low programming voltage anti-fuse	438/132	257/E23.147; 438/131;		Iyer, S. Sundar Kumar et al.	☑	☐	☐	☐	☐	☐	☐	US
19	☐	☐	US 6037620 A	20000314	13	DRAM cell with transfer device extending along perim	257/296	257/301; 257/302;		Hoenigschmid, Heinz et al.	☑	☐	☐	☐	☐	☐	☐	US
20	☐	☐	US 6018174 A	20000125	18	Bottle-shaped trench capacitor with epi buried la	257/296	257/301; 257/309;		Schrems, Martin et al.	☑	☐	☐	☐	☐	☐	☐	US
21	☐	☑	US 6008104 A	19991228	30	Method of fabricating a trench capacitor with a depo	438/386	257/E21.651; 438/243;		Schrems, Martin	☑	☐	☐	☐	☐	☐	☐	US
22	☐	☑	US 5981332 A	19991109	10	Reduced parasitic leakage in semiconductor devices	438/246	257/E27.092; 438/242;		Mandelman, Jack A. et al.	☑	☐	☐	☐	☐	☐	☐	US
23	☐	☑	US 5945704 A	19990831	18	Trench capacitor with epi buried layer	257/301	257/296		Schrems, Martin et al.	☑	☐	☐	☐	☐	☐	☐	US
24	☐	☐	US 5909044 A	19990601	9	Process for forming a high density semiconductor device	257/301	257/303; 257/E21.651		Chakravarti, Ashima Bhattacharyya et al.	☑	☐	☐	☐	☐	☐	☐	US
25	☐	☐	US 5362663 A	19941108	11	Method of forming double well substrate plate trench	438/241	257/E27.092; 438/243		Bronner, Gary B. et al.	☑	☐	☐	☐	☐	☐	☐	US
26	☐	☐	US 5264716 A	19931123	12	Diffused buried plate trench dram cell array	257/301	257/304; 257/311;		Kenney, Donald M.	☑	☐	☐	☐	☐	☐	☐	US
27	☐	☐	US 5250829 A	19931005	11	Double well substrate plate	257/301	257/305; 257/549;		Bronner, Gary B. et al.	☑	☐	☐	☐	☐	☐	☐	US



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P					In
2	☐	☐	US 20030094608 A1	20030522	35	Test structure and methodology for semiconducto	257/48			Abadeer, Wagdi W. et al.	☑	☐	☐	☐	☐	☐	☐	US 20
4	☐	☐	US 20030082875 A1	20030501	20	METHOD OF FORMING A DEEP TRENCH DRAM CELL	438/243	438/241		Lee, Brian	☑	☐	☐	☐	☐	☐	☐	US 20
5	☐	☐	US 20030057483 A1	20030327	19	GROOVED PLANAR DRAM TRANSFER DEVICE USING BURIED POCKET	257/330	257/E21.655		BRONNER, GARY et al.	☑	☐	☐	☐	☐	☐	☐	US 20
6	☐	☑	US 20020132423 A1	20020919	8	Method of forming a uniform collar oxide layer over an u	438/243			Tsao, Li-Wu	☑	☐	☐	☐	☐	☐	☐	US 20
7	☐	☐	US 20010004540 A1	20010621	19	Grooved planar DRAM transfer device using buried pocket	438/270	257/330; 257/E21.655		Bronner, Gary et al.	☑	☐	☐	☐	☐	☐	☐	US 20
8	☐	☐	US 6656807 B2	20031202	20	Grooved planar DRAM transfer device using buried pocket	438/296	438/424; 438/430;		Bronner, Gary et al.	☑	☐	☐	☐	☐	☐	☐	US
9	☐	☐	US 6639264 B1	20031028	7	Method and structure for surface state passivation to	257/301	257/302; 257/305;		Loh, Stephen K.	☑	☐	☐	☐	☐	☐	☐	US
10	☐	☐	US 6614074 B2	20030902	19	Grooved planar DRAM transfer device using buried pocket	257/330	257/332; 257/334;		Bronner, Gary et al.	☑	☐	☐	☐	☐	☐	☐	US
11	☐	☐	US 6551895 B1	20030422	10	Metal oxide semiconductor capacitor utilizing dummy li	438/396	257/E21.396; 257/E27.097;		Hsu, Louis L. et al.	☑	☐	☐	☐	☐	☐	☐	US
12	☐	☑	US 6551875 B2	20030422	8	Method of forming a uniform collar oxide layer over an u	438/246	438/243; 438/240;		Tsao, Li-Wu	☑	☐	☐	☐	☐	☐	☐	US
13	☐	☐	US 6451640 B1	20020917	11	Process for buried-strap self-aligned to deep storage	438/243	257/E21.651; 438/248;		Gruening, Ulrike et al.	☑	☐	☐	☐	☐	☐	☐	US
14	☐	☐	US 6444548 B1	20020903	11	Bitline diffusion with halo for improved array threshold	438/525	257/301; 257/E21.345;		Divakaruni, Ramachandra et al.	☑	☐	☐	☐	☐	☐	☐	US
15	☐	☐	US 6426253 B1	20020730	19	Method of forming a vertically oriented device i	438/243	257/E21.551; 257/E21.629;		Tews, Helmut Horst et al.	☑	☐	☐	☐	☐	☐	☐	US
16	☐	☑	US 6417064 B1	20020709	7	Method for treating the surface of a deep trench	438/386	257/296; 257/E21.335;		Lin, Shian-Jyh et al.	☑	☐	☐	☐	☐	☐	☐	US
17	☐	☐	US 6368912 B1	20020409	13	Method of fabricating an isolation structure between	438/248	257/E21.652; 438/242;		Chang, Chi-Han et al.	☑	☐	☐	☐	☐	☐	☐	US
18	☐	☑	US 6362040 B1	20020326	13	Reduction of orientation dependent oxidation for vert	438/246	257/E21.285; 257/E21.652;		Tews, Helmut Horst et al.	☑	☐	☐	☐	☐	☐	☐	US
19	☐	☐	US 6355518 B1	20020312	8	Method for making a DRAM cell with deep-trench capaci	438/246	257/E21.652; 438/243;		Wu, Chao-chueh et al.	☑	☐	☐	☐	☐	☐	☐	US
20	☐	☐	US 6037194 A	20000314	27	Method for making a DRAM cell with grooved transfer d	438/147	257/E21.655; 438/175		Bronner, Gary B. et al.	☑	☐	☐	☐	☐	☐	☐	US